

REMARKS

Claims 1-20 are pending in the present application. Claims 1-4 are independent. Claims 13 and 17 have been cancelled without prejudice or disclaimer of the subject matter contained therein. Claims 3 and 4 have been amended to include the recitations of canceled claims 13 and 17. Claims 1, 2, 16, and 20 have been amended to make them more readable. As such, the claim amendments do not add new matter or raise new issues.

Claims 1-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Surlekar. Applicant respectfully traverses.

Initially, Applicant notes that the Examiner in the associated Office Action never addressed one of the characteristics of the internal signals of claims 1 and 2 being for controlling internal operations of the integrated circuit. Applicant asserts that Surlekar also fails to disclose this characteristic of the internal operations as recited in claims 1-4 of the present response, and for this reason alone, Surlekar fails to anticipate the recited invention.

With regard to independent claims 1, 3, and 4, Applicant asserts that Surlekar fails to disclose a data output buffer for transferring internal integrated circuit signals externally through data input/output pads; wherein the internal signals are used for addressing storage locations and for controlling internal operations of the integrated circuit as recited in claims 1, 3, and 4. Applicant asserts that Surlekar's output of data through its Data Output Buffer 16 and Data Out Register 17 is different from the signals for controlling internal operations as recited in independent claims 1, 3, and 4. The Surlekar data is data that is stored in a memory, retrieved, and then compared as disclosed at Col. 2, lines 37-44. The Surlekar data is not used for controlling internal operations. Thus, Surlekar fails to disclose a data output buffer that transfers internal signals external to an

integrated circuit device through data input/output pads; the internal signals used for addressing storage locations and for controlling internal operations as recited in claims 1, 3, and 4.

With regard to independent claim 2, Applicant asserts that Surlekar fails to disclose a selection circuit for receiving internal signals in response to selection signals corresponding to test information signals where the internal signals are used for addressing storage locations and for controlling internal operations. Instead, Surlekar discloses a selection circuit 35 for retrieval of data signals from individual cells of a storage array as shown in Fig. 3. Applicant asserts that the data signals of Surlekar are not in response to selection signals corresponding to test information signals. Furthermore, Applicant asserts that the data signals of Surlekar are not used for addressing storage locations and for controlling internal operations. Thus, Applicant contends that Surlekar can not disclose a selection circuit for receiving internal signals in response to selection signals corresponding to test information signals where the internal signals are used for addressing storage locations and for controlling internal operations.

For at least the above reasons, Applicant asserts that Surlekar fails to disclose each and every element of independent claims 1-4 as is required for a 35 U.S.C. § 102 rejection. Accordingly, Applicant asserts that independent claims 1-4 are allowable, and respectfully requests that the 35 U.S.C. § 102 rejection of claims 1-4 be withdrawn.

With regard to claims 13 and 17, applicant asserts that the rejection is moot given the cancellation of claims 13 and 17.

With regard to dependent claims 5-12, 14-16, and 18-20, Applicant asserts that they are allowable for their own merits and at least because they depend from at least one of independent claims 1-4, which the Applicant believes have been shown to be allowable. Accordingly, Applicant respectfully requests that the 35 U.S.C. § 102 rejection of claims 1-20 be withdrawn.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-12, 14-16, and 18-20 are patentable, and that the application as a whole is in condition for allowance. Early and favorable notice to that effect is respectfully solicited.

In the event that any matters remain at issue in the application, the Examiner is invited to contact the undersigned at (703) 668-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C.

By



John A. Castellano
Reg. No. 35,094
P.O. Box 8910
Reston, VA 20195
(703) 668-8000

JAC/RFS